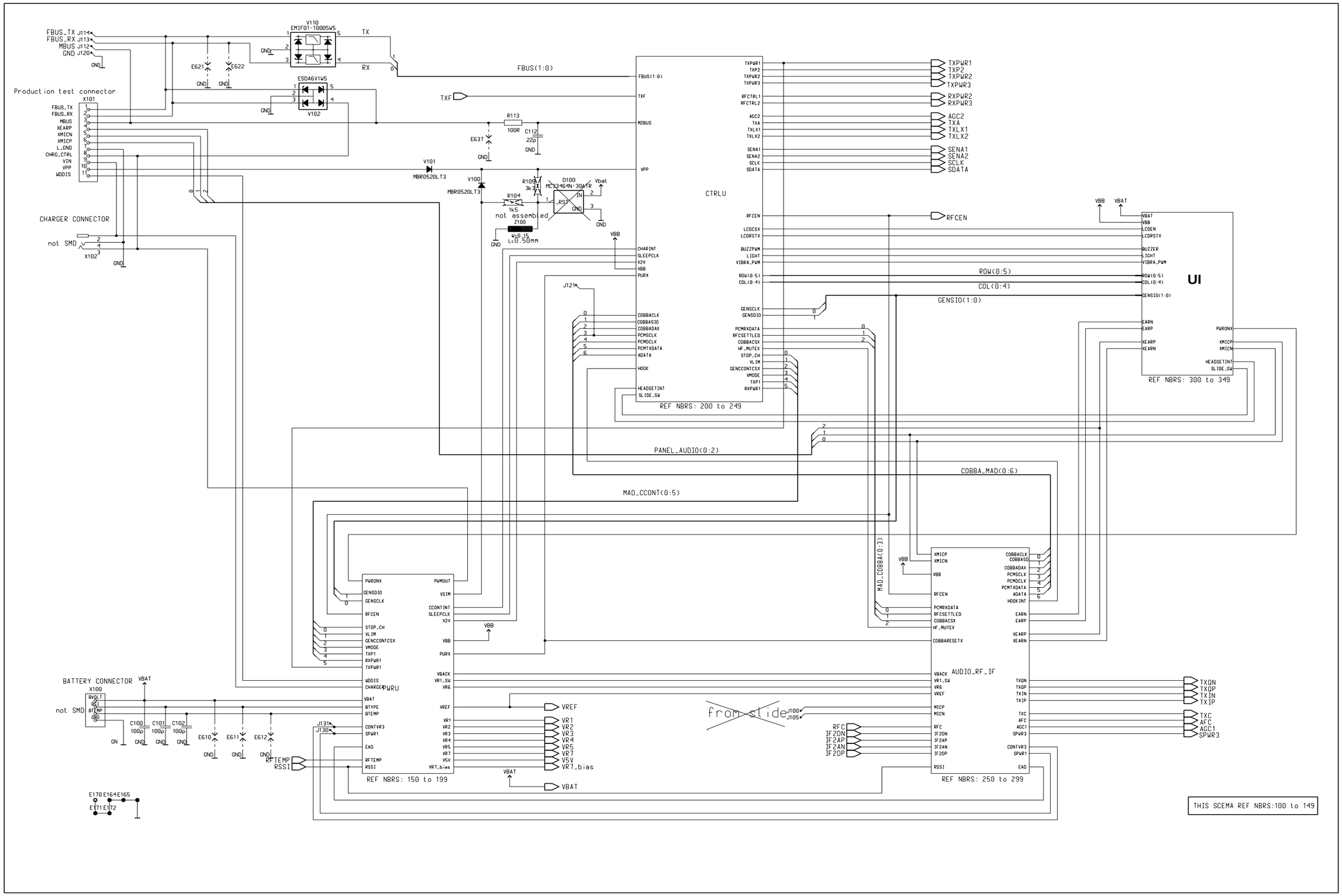
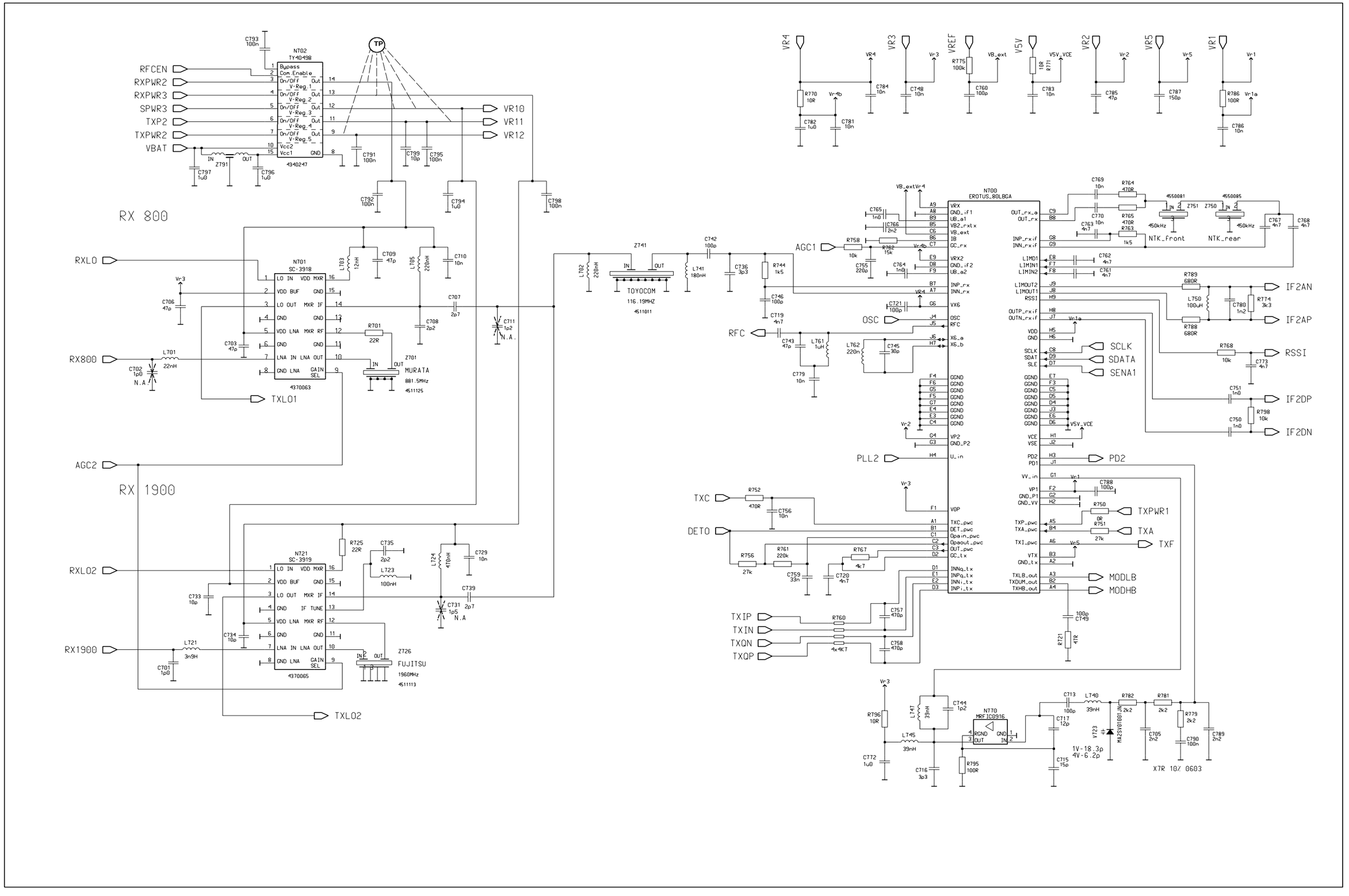
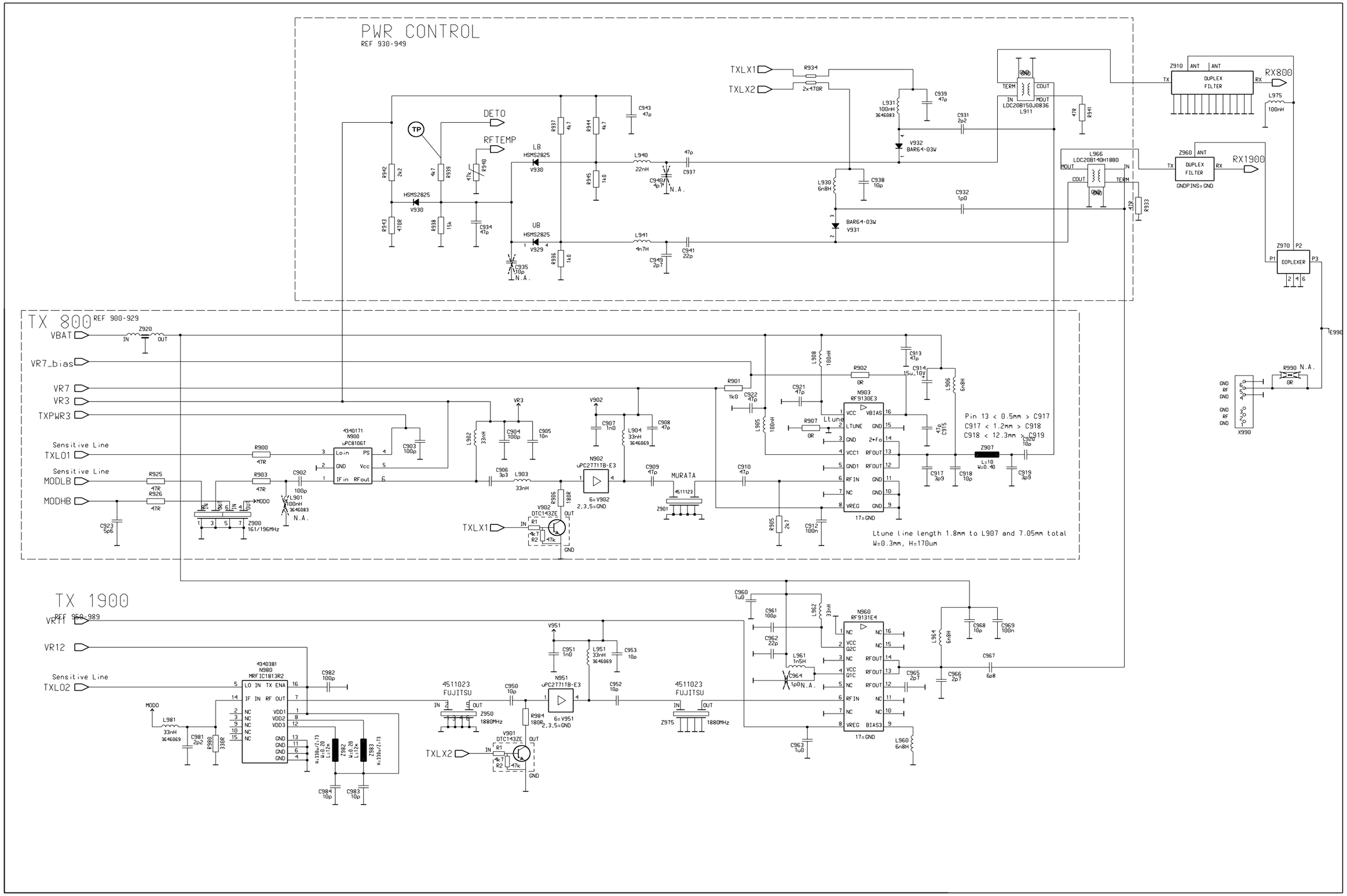
System Block Diagram



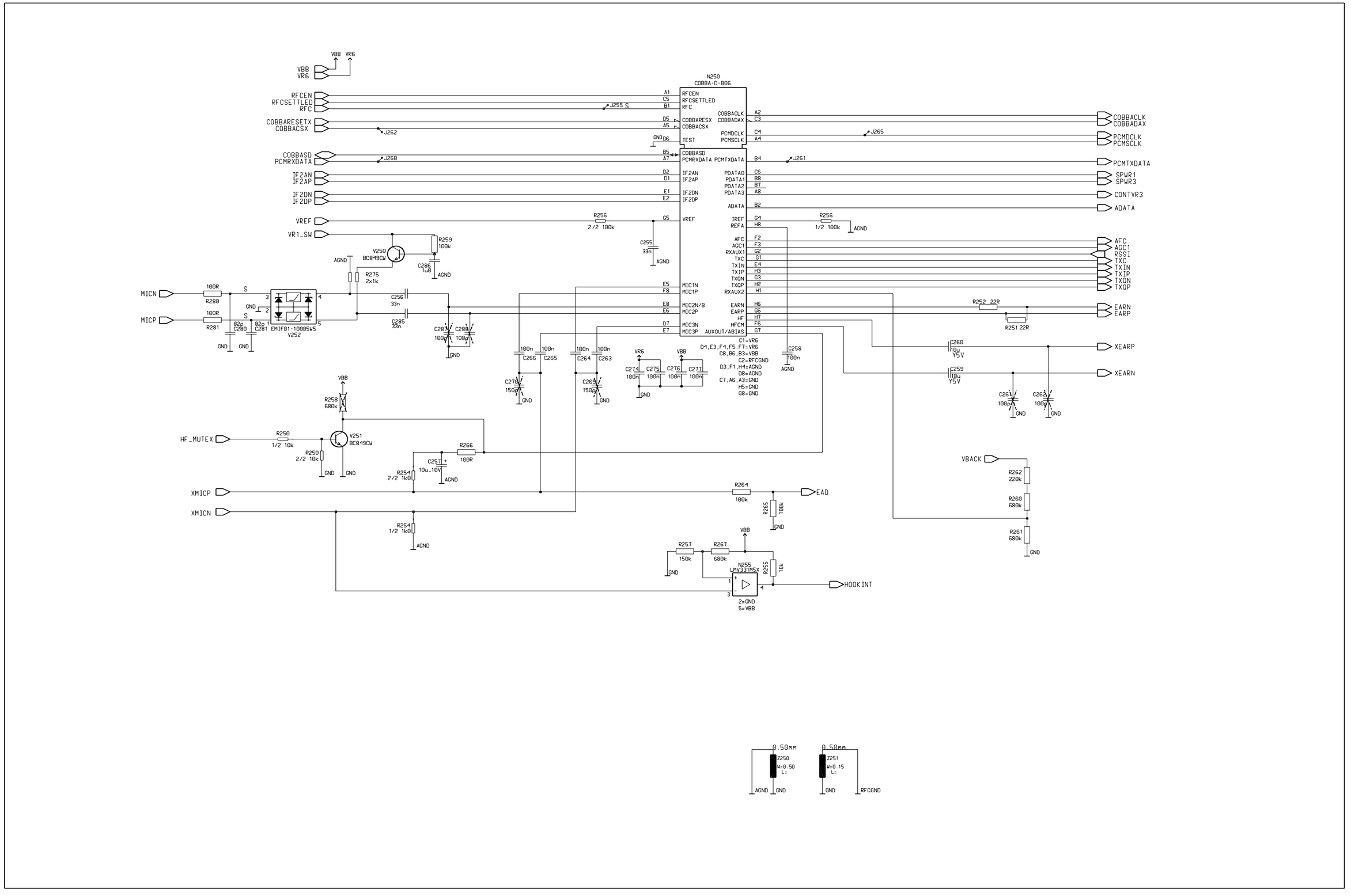
Dualband RX


RX 800
RX 1900
RFCEN
RXPWR2
RXPWR3
SPWR3
TXP2
TXPWR2
VBAT
VR10
VR11
VR12
N702
TY40498
4340247
RXLO
RXL02
RX800
RX1900
AGC2
TXL01
TXL02
N701
SC-3918
4370063
N721
SC-3919
4370065
TOYOCOM
116.19MHZ
4511011
MURATA
881.5MHz
4511125
FUJITSU
1960MHz
4511113
N700
EROTUS_80LBGA
AGC1
OSC
RFC
PLL2
TXC
DETO
TXIP
TXIN
TXQN
TXQP
NTK_front
NTK_rear
IF2AN
IF2AP
RSSI
IF2DP
IF2DN
SCLK
SDATA
SENA1
PD2
TXPWR1
TXA
TXF
MODLB
MODHB
N770
MRFIC0916
X7R 10/ 0603

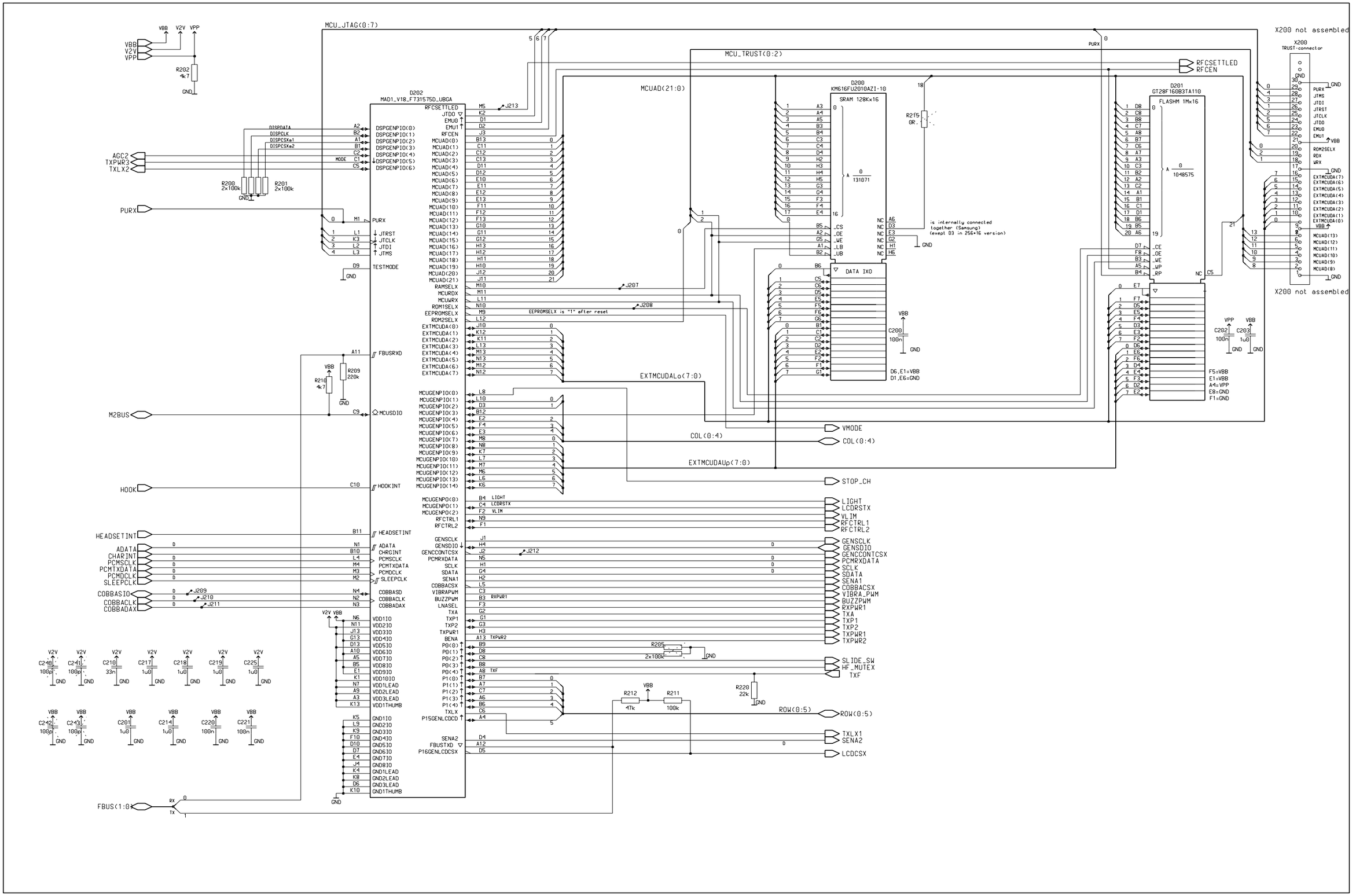
Dualband TX


PWR CONTROL
REF 930-949
TXLX1
TXLX2
R934
2x47OR
DETO
RFTEMP
TP
LB
HSMS2825
V930
UB
HSMS2825
V929
L940
22nH
L941
4n7H
C940
4p7
N.A.
C935
10p
N.A.
C937
47p
C939
47p
C931
2n2
C938
10p
C932
1p0
L931
100nH
3646083
L930
6n8H
V932
BAR64-03W
BAR64-03W
V931
L966
LDC20B140H1880
L911
LDC20B150J0836
Z910
DUPLEX FILTER
RX800
L975
100nH
Z960
DUPLEX FILTER
RX1900
GNDPINS=GND
Z970
DIPLEXER
E990
R990 N.A.
X990
TX 800
REF 900-929
VBAT
Z920
VR7_bias
VR7
VR3
TXPWR3
Sensitive Line
TXLO1
Sensitive Line
MODLB
MODHB
MODO
R900
R925
R926
R903
C902
L901
100nH
3646083
N.A.
Z900
161/196MHz
4340171
N900
uPC8106T
C903
100p
C904
100p
C905
10n
C906
3p3
L903
33nH
N902
uPC2771TB-E3
6=V902
2,3,5=GND
C907
1n0
L904
33nH
3646069
C908
47p
C909
47p
MURATA
4511123
Z901
C910
47p
R985
2k7
C912
100n
R986
180R
V902
DTC143ZE
R1
4k7
R2
47k
GND
C901
100p
R901
1k0
C922
47p
C921
47p
L988
100nH
R902
0R
C913
47p
C914
15u_10V
L986
6n8H
N903
RF9130E3
R907
Ltune
0R
L985
100nH
C915
47p
C916
47p
C917
3p9
C918
10p
C919
3p9
C920
10p
Z907
L=10
W=0.40
Pin 13 < 0.5mm > C917
C917 < 1.2mm > C918
C918 < 12.3mm > C919
Ltune line length 1.8mm to L907 and 7.05mm total
W=0.3mm, H=170um
C923
5p6
TX 1900
REF 960-989
VR11
VR12
Sensitive Line
TXLO2
4340381
N980
MRFIC1813R2
C982
100p
MODO
L981
33nH
3646069
C981
2p2
R980
330R
Z982
W=0.20
L=12m
Z983
W=0.20
L=12m
C984
10p
C983
10p
V951
C951
1n0
L951
33nH
3646069
C953
10p
4511023
FUJITSU
C950
10p
N951
uPC2771TB-E3
6=V951
2,3,5=GND
C952
10p
4511023
FUJITSU
Z950
1880MHz
Z975
1880MHz
R984
180R
V901
DTC143ZE
R1
4k7
R2
47k
GND
TXLX2
C960
1u0
C961
100p
L962
33nH
C962
22p
L961
1n5H
C964
1p0
N.A.
N960
RF9131E4
C963
1u0
L960
6n8H
C965
2p7
L964
6n8H
C966
2p7
C967
6p8
C968
10p
C969
100n

Audio


N250
COBBA-D-B06
VBB
VR6
RFCEN
RFCSETTLED
RFC
COBBARESETX
COBBACSX
COBBASD
PCMRXDATA
IF2AN
IF2AP
IF2DN
IF2DP
VREF
VR1_SW
MICN
MICP
EMIF01-10005W5
V252
V250
BC849CW
V251
BC849CW
HF_MUTEX
XMICP
XMICN
N255
LMV331M5X
HOOK INT
EAD
VBACK
COBBACLK
COBBADAX
PCMDCLK
PCMSCLK
PCMTXDATA
SPWR1
SPWR3
CONTVR3
ADATA
AFC
AGC1
RSSI
TXC
TXIN
TXIP
TXQN
TXQP
EARN
EARP
XEARP
XEARN
AGND
GND
RFCGND
Z250
W=0.50
L=
Z251
W=0.15
L=
0.50mm

CTRLU



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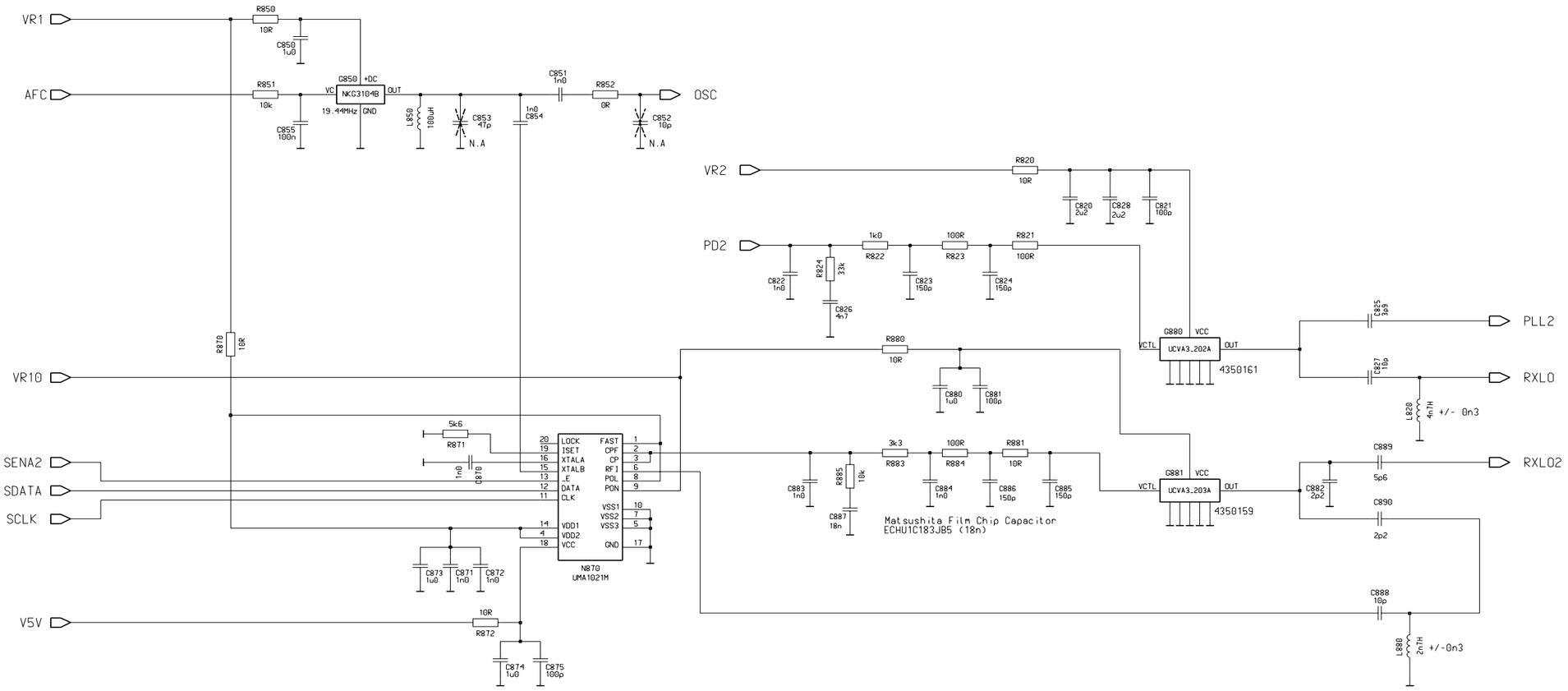
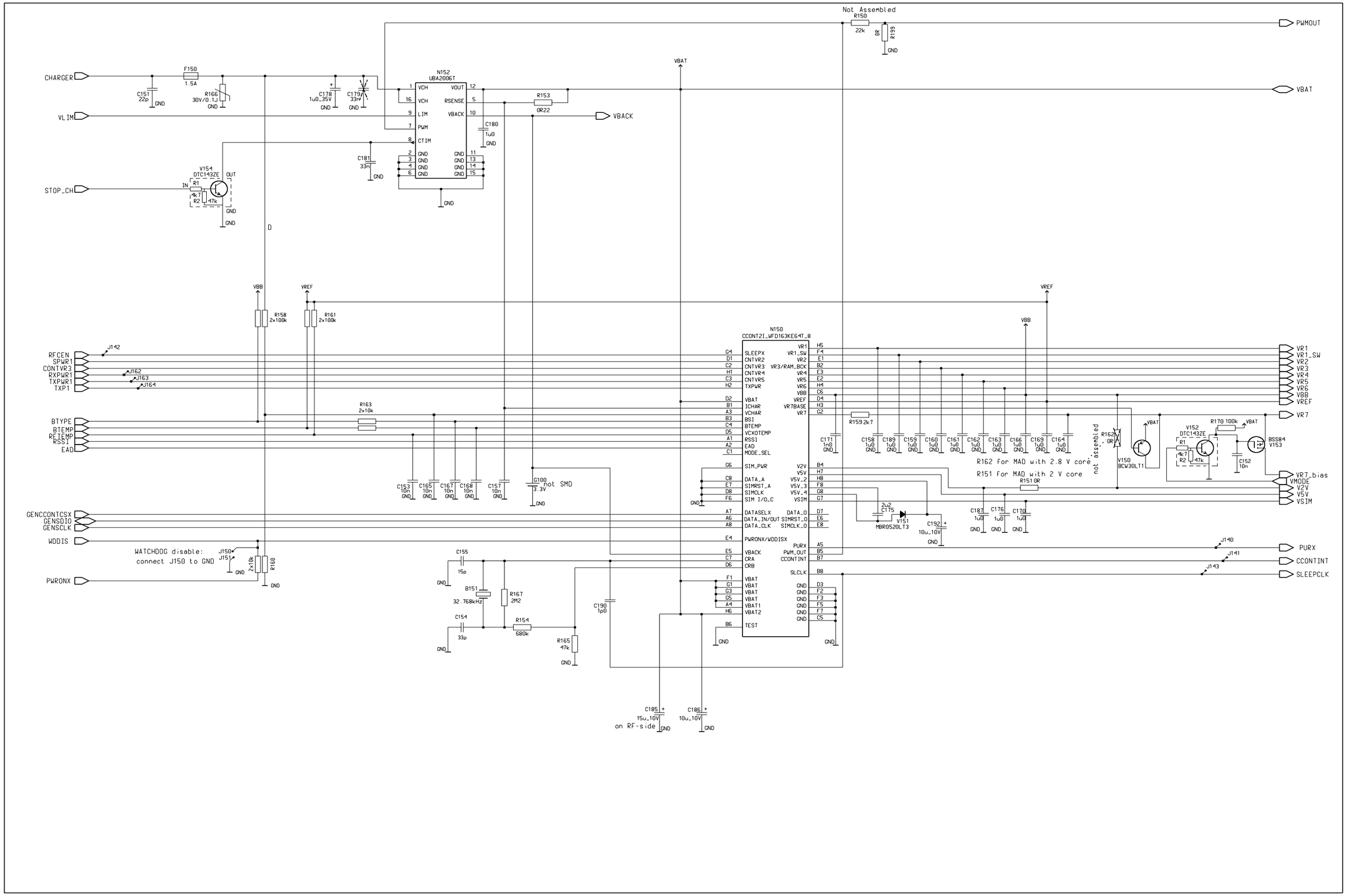
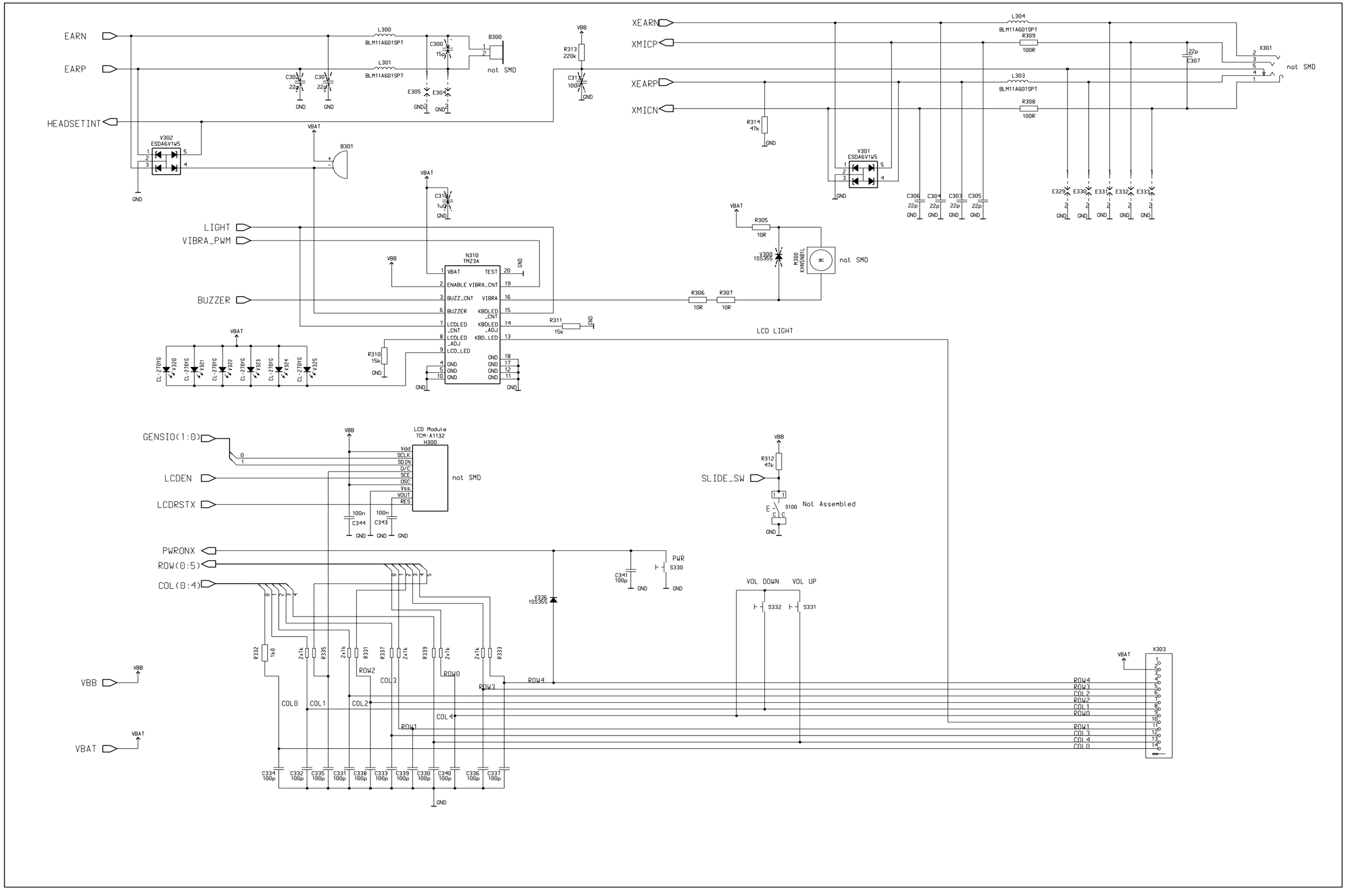
Dualband Synth



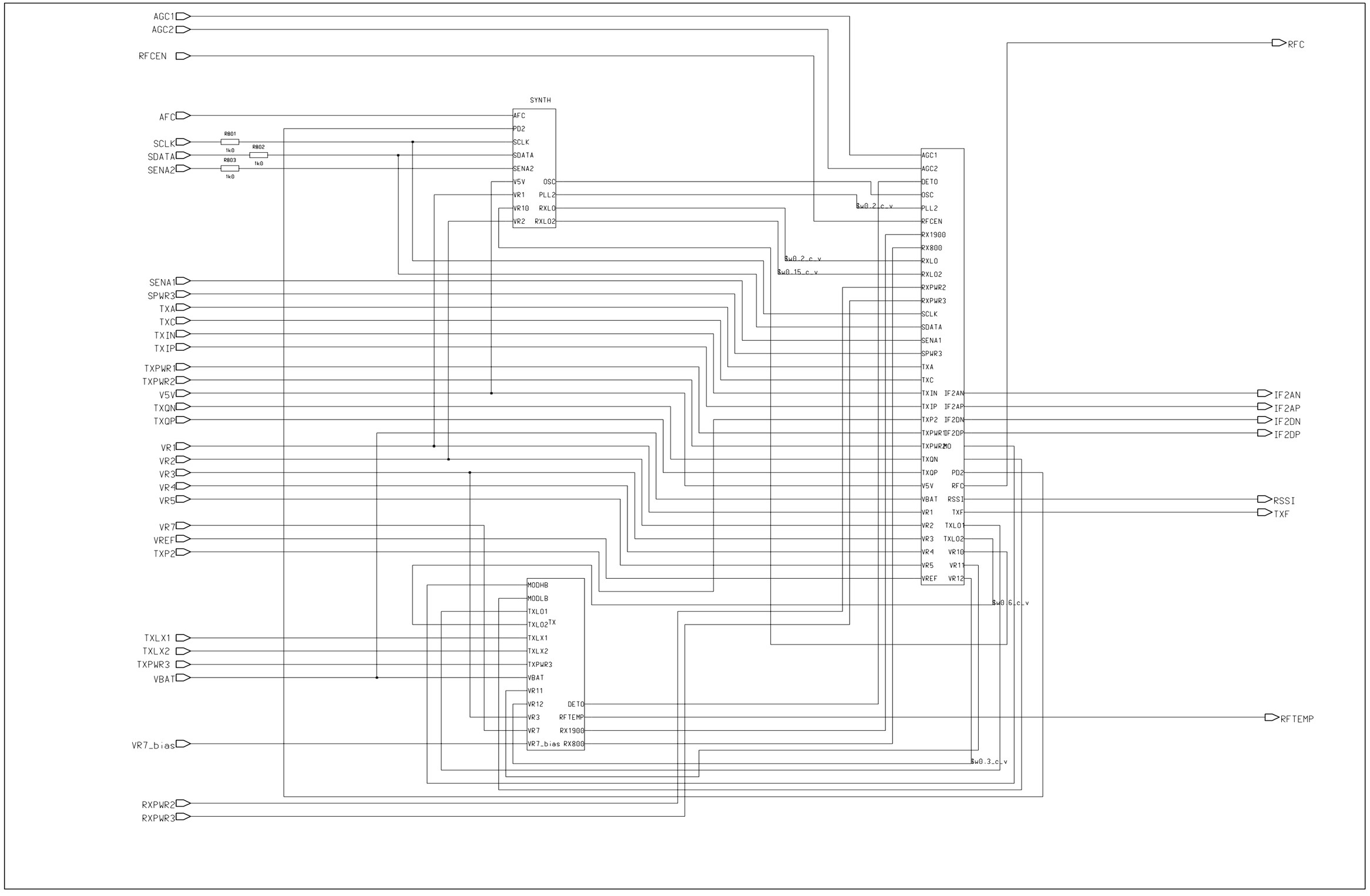
PWRU


Not Assembled
R150
22k
R199
0R
GND
PWMOUT
VBAT
CHARGER
F150
1.5A
C151
22p
R166
30V/0.1J
C178
1u0_35V
C179
33n
N152
UBA2006T
VCH
VCH
LIM
PWM
CTIM
GND
VOUT
RSENSE
VBACK
R153
0R22
VBACK
VLIM
C180
1u0
C181
33n
V154
DTC143ZE
STOP_CH
R1
4k7
R2
47k
D
VBB
VREF
R158
2x100k
R161
2x100k
J142
RFCEN
SPWR1
CONTVR3
RXPWR1
TXPWR1
TXP1
J162
J163
J164
R163
2x10k
BTYPE
BTEMP
RTEMP
RSSI
EAD
C153
10n
C165
10n
C167
10n
C168
10n
C157
10n
C100
not SMD
3.3V
GENCCONTCSX
GENSDIO
GENSCLK
WDDIS
PWRONX
WATCHDOG disable:
connect J150 to GND
J150
J151
2x10k
R160
C155
15p
B151
32.768kHz
R167
2M2
C154
33p
R154
680k
R165
47k
C190
1p0
C185
15u_10V
on RF-side
C186
10u_10V
N150
CCONT2I_WFD163KE64T_8
SLEEPX
CNTVR2
CNTVR3
CNTVR4
CNTVR5
TXPWR
VBAT
ICHAR
VCHAR
BSI
BTEMP
VCXOTEMP
RSSI
EAD
MODE_SEL
SIM_PWR
DATA_A
SIMRST_A
SIMCLK
SIM I/O_C
DATASELX
DATA_IN/OUT
DATA_CLK
PWRONX/WDDISX
VBACK
CRA
CRB
VBAT
VBAT
VBAT
VBAT
VBAT1
VBAT2
TEST
VR1
VR1_SW
VR2
VR3/RAM_BCK
VR4
VR5
VR6
VBB
VREF
VR7BASE
VR7
V2V
V5V
V5V_2
V5V_3
V5V_4
VSIM
DATA_O
SIMRST_O
SIMCLK_O
PURX
PWM_OUT
CCONTINT
SLCLK
GND
R1592k7
C171
1u0
C158
1u0
C189
1u0
C159
1u0
C160
1u0
C161
1u0
C162
1u0
C163
1u0
C166
1u0
C169
1u0
C164
1u0
R162 for MAD with 2.8 V core
R151 for MAD with 2 V core
R151 0R
not assembled
R162
0R
V150
BCW30LT1
2u2
C175
V151
MBR0520LT3
C192
10u_10V
C187
1u0
C176
1u0
C170
1u0
R170 100k
V152
DTC143ZE
R1
4k7
R2
47k
C152
10n
BSS84
V153
VR1
VR1_SW
VR2
VR3
VR4
VR5
VR6
VBB
VREF
VR7
VR7_bias
VMODE
V2V
V5V
VSIM
J140
J141
J143
PURX
CCONTINT
SLEEPCLK

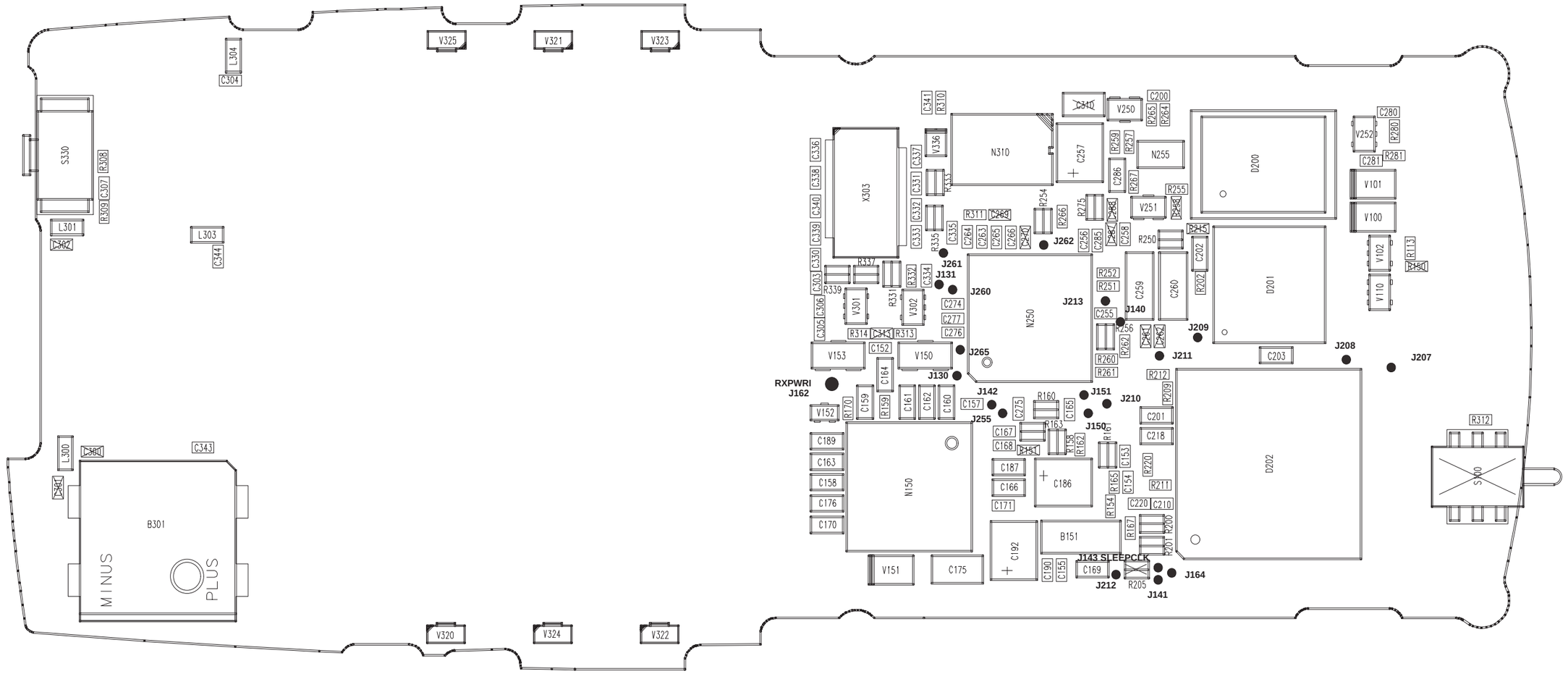
User Interface



Dualband RF


AGC1
AGC2
RFCEN
AFC
SCLK
SDATA
SENA2
R801
1k0
R802
1k0
R803
1k0
SYNTH
AFC
PD2
SCLK
SDATA
SENA2
V5V OSC
VR1 PLL2
VR10 RXLO
VR2 RXLO2
SENA1
SPWR3
TXA
TXC
TXIN
TXIP
TXPWR1
TXPWR2
V5V
TXQN
TXQP
VR1
VR2
VR3
VR4
VR5
VR7
VREF
TXP2
MODHB
MODLB
TXLO1
TXLO2TX
TXLX1
TXLX2
TXPWR3
VBAT
VR11
VR12 DETO
VR3 RFTEMP
VR7 RX1900
VR7_bias RX800
TXLX1
TXLX2
TXPWR3
VBAT
VR7_bias
RXPWR2
RXPWR3
AGC1
AGC2
DETO
OSC
PLL2
RFCEN
RX1900
RX800
RXLO
RXLO2
RXPWR2
RXPWR3
SCLK
SDATA
SENA1
SPWR3
TXA
TXC
TXIN IF2AN
TXIP IF2AP
TXP2 IF2DN
TXPWR1IF2DP
TXPWR2MO
TXQN
TXQP PD2
V5V RFC
VBAT RSSI
VR1 TXF
VR2 TXLO1
VR3 TXLO2
VR4 VR10
VR5 VR11
VREF VR12
RFC
IF2AN
IF2AP
IF2DN
IF2DP
RSSI
TXF
RFTEMP
Sw0.2_c_v
Sw0.2_c_v
Sw0.15_c_v
Sw0.6_c_v
Sw0.3_c_v

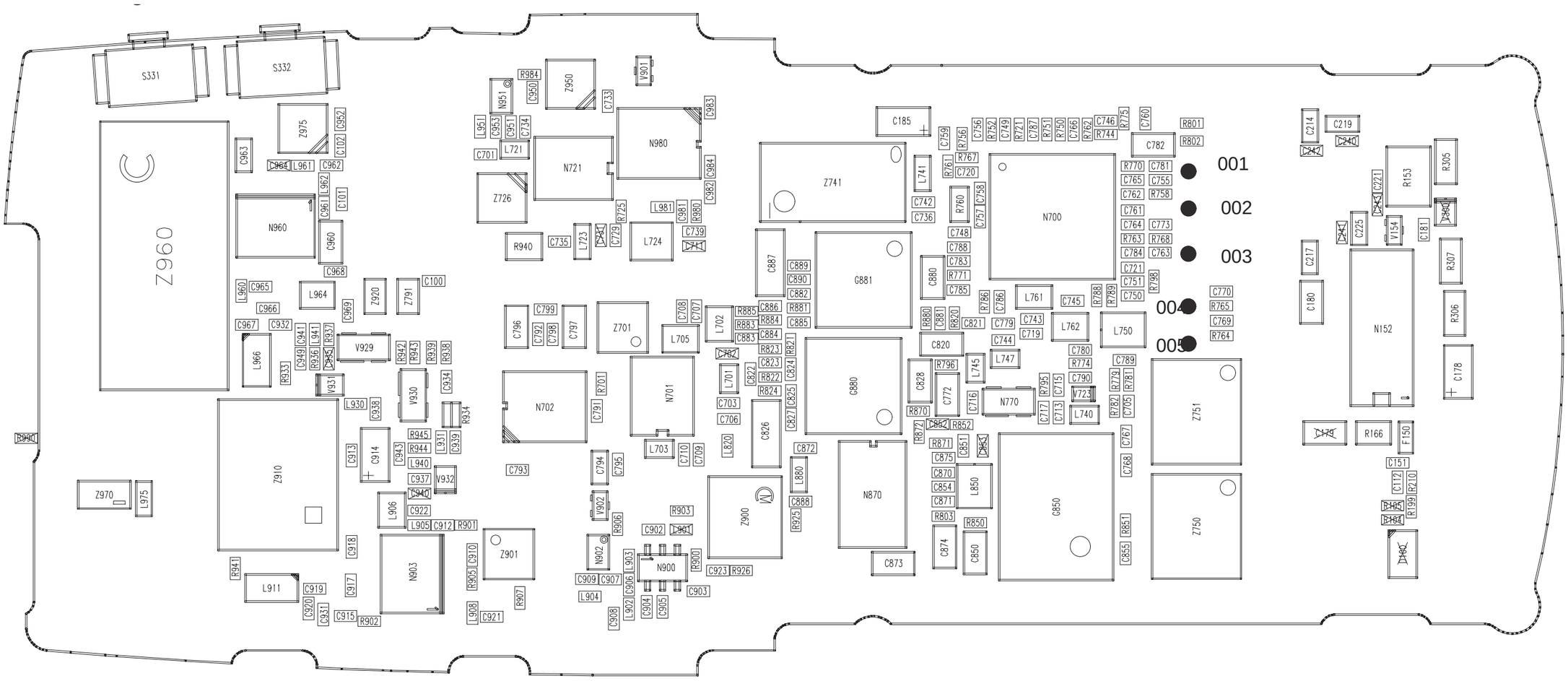
Component Layout - Top



Test point description				
Test point	**Name**	**From–to**	**Level**	**Description**
J121	PCMSCLK	COBBA A4– MAD L4		8.0 kHz (digital), 8.1 kHz (analog)
J140	PURX	CCONT A5–MAD M1, D201 B4, COBBA D5	Reset state 0V, normal state 2.8V	RESET power up/down
J141	CCONTINT	CCONT B7–MAD B10	Pulse active 2.8V, non–active 0V	Charger interrupt
J142	RFCEN	MAD J3– D201 A5, CCONT G4	Pulse active 2.8V, non–active 0V	Active state
J143	SLEEPCLK	CCONT B8– MAD M2	Pulsed DC < 0.8V/>2.4V	32.768 kHz, power on
J150	WDDIS/PWRONX	X101–CCONT E4	Pulse active 0V, non–active 2.8V	Watchdog disable
J151	GND	J156–GND		Ground for WDDIS

J207	RAMSELX	MAD M10– D200 B5		
J208	ROM1SELX	MAD N10– D201 D7		
J209	COBBASIO	MAD N4– COBBA B5		Bidirectional data line
J210	COBBACLK	COBBA A2– MAD N2	Pulsed DC (<0.5V/>2.15V)	COBBA system clock
J211	COBBADAX	MAD N3– COBBA C3		Data ready flag
J212	DATASELX	MAD J2– CCONT A7		Read/write enable
J213	RFCSETTLED	MAD M5– COBBA C5	Pulse active 2.8V, non–active 0 V	Active state
J262	COBBACSX	MAD L5– COBBA A5		Chip select
J255	RFC	EROTUS 25– COBBA B1	0.7 Vpp sinewave	19.44 MHz clock
J260	PCMRXDATA	MAD N5– COBBA A7		Receive data line
J261	PCMTXDATA	COBBA B4– MAD M4		Transmit data line
J265	PCMDCLK	COBBA C4– MAD M3		1.08 MHz (digital), 1.215 MHz (analog)

Component Layout - Bottom



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